CFP2-27B4-10D-RX

100 Gb/s CFP2 LR4 Receiver

PRODUCT FEATURES

- Compliant with 100GBASE-LR4
- Support line rates from 103.125 Gbps to 111.81 Gbps
- Integrated LAN WDM ROSA for up to 10 km reach over SMF
- Digital Diagnostics Monitoring Interface
- Duplex LC optical receptacle
- No external reference clock and Single 3.3 V power supply
- Case operating temperature range:0°C to 70°C
- Power dissipation < 2 W

APPLICATIONS

- Data Center &100G Ethernet
- ITU-T OTU4

STANDARD

- Compliant to IEEE 802.3ba
- Compliant to CFP MSA CFP2 Hardware Specification
- Compliant to CFP MSA CFP2 Management Interface Specification

General Description

XGIGA 100G CFP2 LR4 receiver integrates receiver path on one module. In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a PIN photo-detector and trans-impedance amplifier, retimed. This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

The module provides an aggregated signaling rate from 103.125 Gbps to 111.81 Gbps. It is compliant with IEEE 802.3-2012 Clause 88 100GBASE-LR4 and ITU-T G.959.1-2012-02, and OIF2010.404.08 CEI-28G-VSR electrical specifications. The MDIO management interface complies with IEEE 802.3-2012 Clause 45 standard. The transceiver complies with CFP MSA CFP2 Hardware Specification Rev. 1.0, CFP MSA Management Interface Specification Rev. 2.2, and OIF CEI-28G-VSR standards.

Receiver

The receiver takes incoming combined four lanes optical data from line rate of 25.78 Gbps to 27.95 Gbps through an industry standard LC optical connector. The four incoming wavelengths are separated by an optical de-multiplexer into four separated channels. Each output is coupled to a PIN photo-detector. The electrical currents from each PIN photo-detector are converted to a voltage with a high-gain transimpedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output to RDxp and RDxn pins.

Low Speed Signaling

Low speed signaling is based on low voltage CMOS (LVCMOS) operating at a nominal voltage of 3.3 V for the control and alarm signals, and at a nominal voltage of 1.2 V for MDIO address, clock and data signals. All low speed inputs and outputs are based on the CFP MSA CFP2 Hardware Specification Rev. 1.0 and CFP MSA Management Interface Specification Rev. 2.2 requirements.

MDC/MDIO: Management interface clock and data lines.

PRTADR0, 1, 2: Input pins. MDIO physical port addresses.

GLB_ALEMn: Output pin. When asserted low indicates that the module has detected an alarm condition in any MDIO alarm register.

PRG_CNTL1, 2, 3: Input pins. Programmable control lines defined in the CFP MSA Management

Interface Specification. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

TX_Disable: Input pin. When asserted high or left open the transmitter output is turned off. When Tx_Dsiable is asserted low or grounded the module transmitter is operating normally. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

MOD_LOPWR: Input pin. When asserted high or left open the CFP2 module is in low power mode. When asserted low or grounded the module is operating normally. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

MOD_RSTn: Input pin. When asserted low or grounded the module is in Reset mode. When asserted high or left open the CFP2 module is operating normally after an initialization process. Pulled down with 4.7 kΩ to 10 kΩ resistors to ground inside the CFP2 module.

PRG_ALRM1, 2, 3: Output pins. Programmable alarm lines defined in the CFP MSA Management Interface Specification.

Mod_ABS: Output pin. Asserted high when the CFP2 module is absent and is pulled low when the CFP2 module is inserted.

RX_LOS: Output pin. Asserted high when insufficient optical power for reliable signal reception is received.

Pin Function Definitions

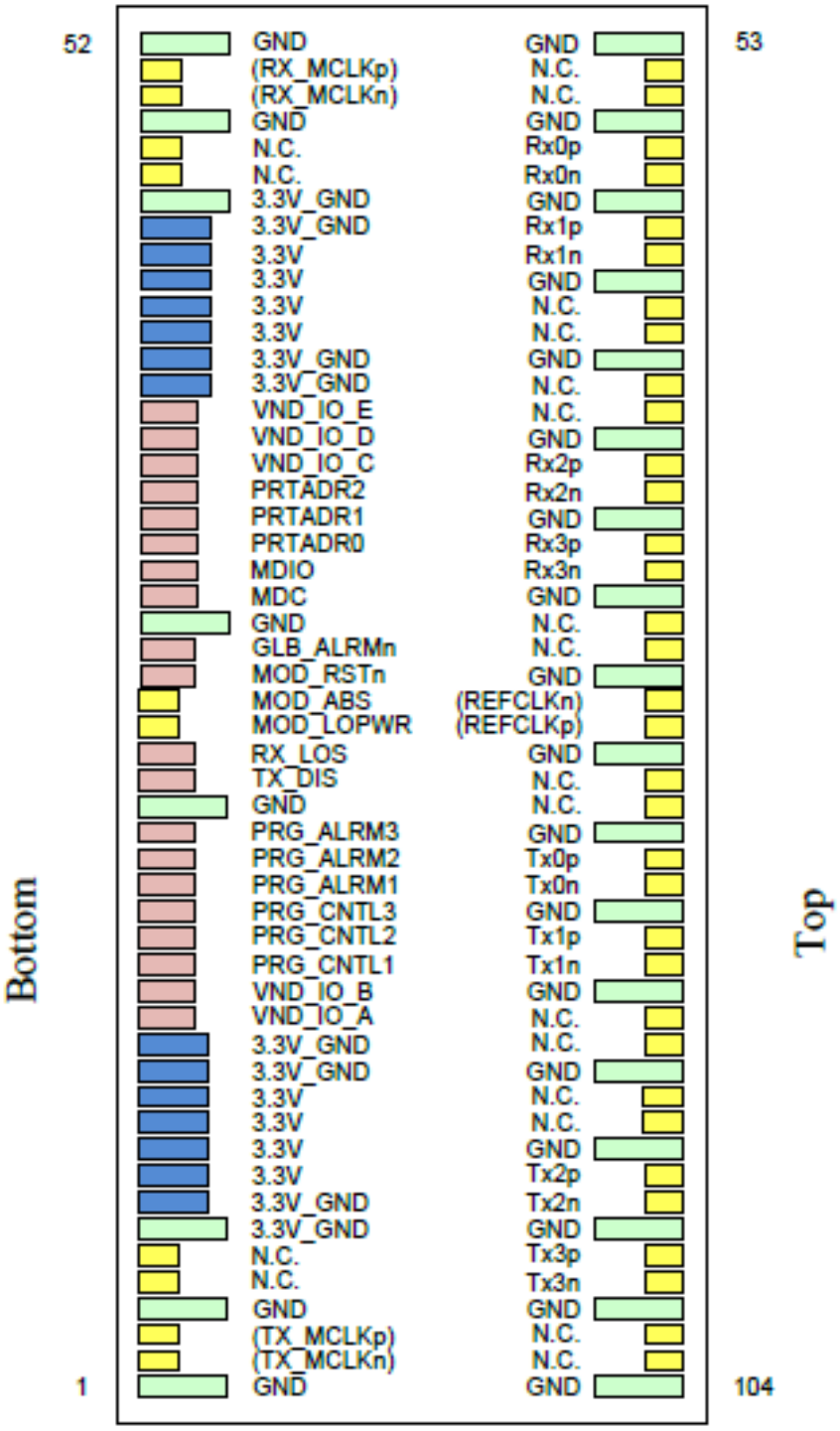

Figure 2 CFP2 optical transceiver pin-out

Table 1 CFP2 optical transceiver pin descriptions

Pin no.	Type	Name	Description
1		GND	Module ground
2	CML	(TX_MCLKn)	No connect
3	CML	(TX_MCLKp)	No connect
4		GND	Module ground
5		N.C.	No connect
6		N.C.	No connect
7		3.3V_GND	3.3V ground; tied with module ground
8		3.3V_GND	3.3V ground; tied with module ground
9		3.3V	3.3V module supply voltage
10		3.3V	3.3V module supply voltage
11		3.3V	3.3V module supply voltage
12		3.3V	3.3V module supply voltage
13		3.3V_GND	3.3V ground; tied with module ground
14		3.3V_GND	3.3V ground; tied with module ground
15		VND_IO_A	Module vendor IO A; do not connect
16		VND_IO_B	Module vendor IO B; do not connect
17	LVCMOS1	PRG_CNTL1	Programmable control 1; MSA default: TRXIC_RSTn; “0”: reset; “1” or NC: not used
18	LVCMOS1	PRG_CNTL2	Programmable control 2; MSA default: Hardware interlock LSB; Default “0”: ≤ 9 W
19	LVCMOS1	PRG_CNTL3	Programmable control 3: MSA default: Hardware interlock MSB; Default “1”: ≤ 9 W
20	LVCMOS	PRG_ALRM1	Programmable alarm 1; MSA default: HIPWR_ON; “1”: module power up completed, “0”: module not high powered up
21	LVCMOS	PRG_ALRM2	Programmable alarm 2; MSA default: MOD_READY, “1”: Ready, “0”: not Ready
22	LVCMOS	PRG_ALRM3	Programmable alarm 3; MSA default:: MOD_FAULT, “1”: Fault, “0”: no Fault
23		GND	Module ground
24	LVCMOS1	TX_DIS	Transmitter disable for all lanes; “1” or NC: transmitter disabled; “0”: transmitter enabled
25	LVCMOS	RX_LOS	Receiver loss of optical signal; “1”: low optical signal, “0”: normal condition
26	LVCMOS1	MOD_LOPWR	Module low power mode; “1” or NC: module in low power mode, “0”: power on enabled
27	GND	MOD_ABS	Module absent; “1” or NC: module absent; “0”: module present. Pull up resistor on host.
28	LVCMOS2	MOD_RSTn	Module reset; “0”: reset the module; “1” or NC: module enabled

Pin no.	Type	Name	Description
29	LVCMOS	GLB_ALRMn	Global alarm; “0”: alarm in any MDIO alarm register; “1”: no alarm condition. Pull up resistor on host.
30		GND	Module ground
31	1.2V CMOS	MDC	Management interface clock input
32	1.2V CMOS	MDIO	Management interface bi-directional data
33	1.2V CMOS	PRTADR0	MDIO physical port address bit 0
34	1.2V CMOS	PRTADR1	MDIO physical port address bit 1
35	1.2V CMOS	PRTADR2	MDIO physical port address bit 2
36		VND_IO_C	Module vendor IO C; do not connect
37		VND_IO_D	Module vendor IO D; do not connect
38		VND_IO_E	Module vendor IO E; do not connect
39		3.3V_GND	3.3V ground; tied with module ground
40		3.3V_GND	3.3V ground; tied with module ground
41		3.3V	3.3V module supply voltage
42		3.3V	3.3V module supply voltage
43		3.3V	3.3V module supply voltage
44		3.3V	3.3V module supply voltage
45		3.3V_GND	3.3V ground; tied with module ground
46		3.3V_GND	3.3V ground; tied with module ground
47		N.C.	No connect
48		N.C.	No connect
49		GND	Module ground
50	CML	(RX_MCLKn)	No connect
51	CML	(RX_MCLKp)	No connect
52		GND	Module ground
53		GND	Module ground
54		N.C.	No connect
55		N.C.	No connect
56		GND	Module ground
57		RX0P	25 Gbps receiver data; Lane 0
58		RX0n	25 Gbps receiver data bar; Lane 0
59		GND	Module ground
60		RX1p	25 Gbps receiver data; Lane 1

Pin no.	Type	Name	Description
61		RX1n	25 Gbps receiver data bar; Lane 1
62		GND	Module ground
63		N.C.	No connect
64		N.C.	No connect
65		GND	Module ground
66		N.C.	No connect
67		N.C.	No connect
68		GND	Module ground
69		RX2p	25 Gbps receiver data; Lane 2
70		RX2n	25 Gbps receiver data bar; Lane 2
71		GND	Module ground
72		RX3p	25 Gbps receiver data; Lane 3
73		RX3n	25 Gbps receiver data bar; Lane 3
74		GND	Module ground
75		N.C.	No connect
76		N.C.	No connect
77		GND	Module ground
78	CML	(REFCLKp)	Module reference clock. No connect.
79	CML	(REFCLKn)	Module reference clock. No connect.
80		GND	Module ground
81		N.C.	No connect
82		N.C.	No connect
83		GND	Module ground
84		TX0p	25 Gbps transmitter data; Lane 0
85		TX0n	25 Gbps transmitter data bar; Lane 0
86		GND	Module ground
87		TX1p	25 Gbps transmitter data; Lane 1
88		TX1n	25 Gbps transmitter data bar; Lane 1
89		GND	Module ground
90		N.C.	No connect
91		N.C.	No connect
92		GND	Module ground

Pin no.	Type	Name	Description
93		N.C.	No connect
94		N.C.	No connect
95		GND	Module ground
96		TX2p	25 Gbps transmitter data; Lane 2
97		TX2n	25 Gbps transmitter data bar; Lane 2
98		GND	Module ground
99		TX3p	25 Gbps transmitter data; Lane 3
100		TX3n	25 Gbps transmitter data bar; Lane 3
101		GND	Module ground
102		N.C.	No connect
103		N.C.	No connect
104		GND	Module ground
1. Pulled up with 4.7 kΩ – 10 kΩ to 3.3 V inside the module.			
2. Pulled down with 4.7 kΩ – 10 kΩ to GND inside the module			

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	℃	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	
Receive Input Optical Power (Damage threshold)	Pdmg			5.0	dBm	

II. Low Speed Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Supply currents and voltages						
Voltage	Vcc	3.2	3.3	3.4	V	With Respect to GND
Supply current	Icc			0.6	A	
Power dissipation	Pwr			2.0	W	
Low speed control and sense signals, 3.3 V LVCMOS						
Outputs low voltage	V_{OL}			0.2	V	I_{OH}=100 µA

Output high voltage	V_{OH}	Vcc-0.2			V	I_{OH}=-100 μA
Low speed control and sense signals, 1.2 V LVCMOS						
Outputs low voltage	V_{OL}	-0.3		0.2	V	
Output high voltage	V_{OH}	1.0		1.5	V	
Output low current	I_{OL}	4			mA	
Output high current	I_{OH}			-4	mA	
MDC clock rate		0.1		4	MHz	

III. High Speed Electrical Specifications

Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Receiver electrical output to host					
Differential voltage pk-pk		100	1200	mV	
Common mode noise (rms)			17.5	mV	
Differential termination mismatch			10	%	
Transition time		9.5		ps	20/80%
Vertical eye closure	VEC		6.5	dB	
Eye width	EW15	0.57		UI	At 10^{-15} probability
Eye height	EH15	240	mV		At 10^{-15} probability

IV. MDIO Management Interface

The XGIGA CFP2 Optical Transceiver incorporates MDIO management interface which is used for serial ID, digital diagnostics, and certain control and status report functions. The CFP2 transceiver supports MDIO pages 8000h NVR 1 Based ID registers, 8080h NVR 2 Extended ID registers, 8100h NVR 3 network lane specific registers , 8180h NVR 4 registers ,and pages A000h module VR 1 registers(module level control and DDM registers)， A200h network lane VR 1 registers，A280h network lane VR 2 registers,A400h host lane VR1 specific registers.

Details of the protocol and interface are explicitly described in CFP MSA Management Interface Specification. Please refer to the specifications for design reference.

Figure 3 CFP2 MDIO Interface

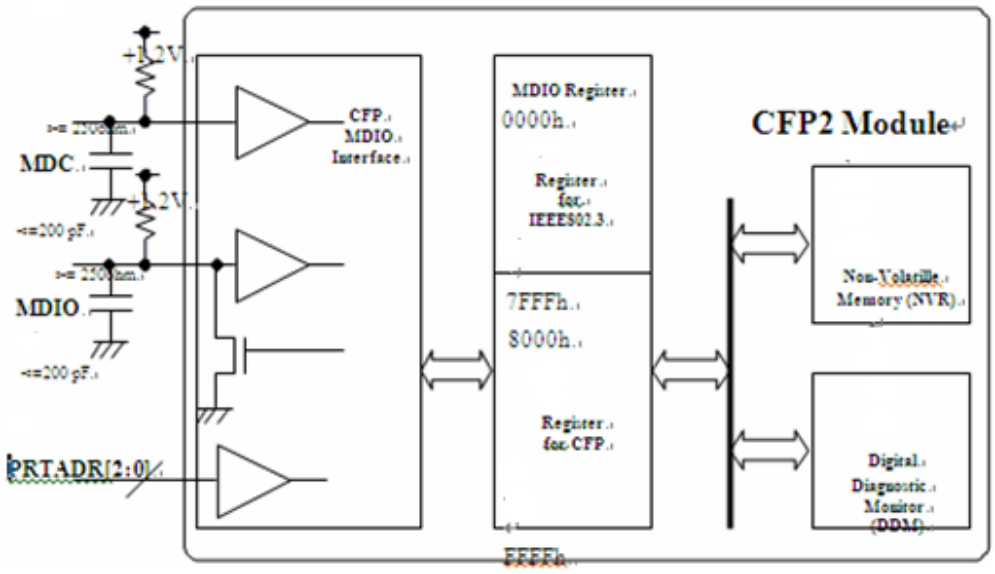

Table 2. CFP2 Register Allocation

Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 Use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA.
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control and DDM registers.
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.

A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA.
B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA.

Table 3. CFP2 NVR 1-- Non-Volatile Register (NVR) Map

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
8000	1	RO		Module Identifier		11h	11: CFP2	N/A
8001	1	RO		Extended Identifier		A4h	10100100	N/A
			7	Power Class	1		10b: Class 3 (=<9W)	N/A
			6		0			N/A
			5	Lane Ratio Type	1		10b: n : n Parallel type	N/A
			4		0			N/A
			3	WDM Type	0		010b: LAN-WDM	N/A
			2		1			N/A
			1		0			N/A
			0	CLEI Presence	0		0: No CLEI code present	N/A
8002	1	RO		Connector Type Code		07h	01h: SC 07h: LC, Angled-LC	N/A
8003	1	RO		Ethernet Application Code		01h	01: 100GBASE-LR4	N/A
8004	1	RO		Fiber Channel Application Code		00h	00h: Undefined type	N/A
8005	1	RO		Copper Link Application Code		00h	00h: Undefined type	N/A
8006	1	RO		SONET/SDH Application Code		00h	00: Undefined type	N/A
8007	1	RO		OTN Application Code		00h	00: Undefined type	N/A
8008	1	RO		Additional Capable Rates Supported		58h	01011000	N/A
			7	Reserved	0		0: Reserved	N/A
			6	OTU4 with Enhanced FEC	1		1: Supported	N/A
			5	OTU3 with Enhanced FEC	0		0: Not supported	N/A
			4	111.8 Gbps	1		1: Supported	N/A
			3	103.125 Gbps	1		1: Supported	N/A
			2	41.25 Gbps	0		0: Not supported	N/A
			1	43 Gbps	0		0: Not supported	N/A
			0	39.8 Gbps	0		0: Not supported	N/A

8009	1	RO		Number of Lanes Supported		44h	01000100	N/A
			7	Number of Network Lanes	0		0100: 4 lanes	N/A
			6		1			
			5		0			
			4		0			
			3	Number of Host Lanes	0		0100: 4 lanes	N/A
			2		1			
			1		0			
			0		0			
800A	1	RO		Media Properties		14h	00010100	N/A
			7	Media Type	0		00b: SM F	N/A
			6		0			
			5	Directionality	0		0: Normal	N/A
			4	Optical Mux and DeMux	1		1: with optical MUX/DEMUX	N/A
			3	Active Fiber per Connector	0		0100b: 4 TX lane and 4 RX lane	N/A
			2		1			
			1		0			
			0		0			
800B	1	RO		Maximum Network Lane Bit Rate		8Ch	8Ch: 27.9529Gbps / 0.2	0.2 Gbps
800C	1	RO		Maximum Host Lane Bit Rate		8Ch	8Ch: 27.9529Gbps / 0.2	0.2 Gbps
800D	1	RO		Maximum Single Mode Optical Fiber		0Ah	0Ah: 10 km	1 km
800E	1	RO		Maximum Multi-M ode Optical Fiber		00h	00h: not supported	10 m
800F	1	RO		Maximum Copper Cable Length		00h	00h: not supported	1 m
8010	1	RO		Transmitter Spectral Characteristics 1		01h	00000001	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	
			5		0		0: Reserved	
			4	Number of Active Transmit Fibers	0		00001b: 1 Fiber	N/A
			3		0			
			2		0			
			1		0			
			0		1			
8011	1	RO		Transmitter Spectral Characteristics 2		04h	00000100	N/A

			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4	Number of Wavelengths per active Transmit Fiber	0		00100b: 4 Wavelengths	N/A
			3		0			N/A
			2		1			N/A
			1		0			N/A
			0		0			N/A
8012	2	RO		Minimum Wavelength per Active Fiber		CAh	CA45h: 1294.53 nm	0.025 nm
8013						45h		
8014	2	RO		Maximum Wavelength per Active Fiber		CCh	CCB8h: 1310.19 nm	0.025 nm
8015						B8h		
8016	2	RO		Maximum per Lane Optical Width		08h	0834h: 2.1 nm	1 pm
8017						34h		
8018	1	RO		Device Technology 1		21h	00100001	N/A
			7	Laser Source Technology	0		0010b: DFB	N/A
			6		0			N/A
			5		1			N/A
			4		0			N/A
			3	Transmitter modulation technology	0		0001b: EML	N/A
			2		0			N/A
			1		0			N/A
			0		1			N/A
8019	1	RO		Device Technology 2		C4h	11000100	N/A
			7	Wavelength control	1		1: Active wavelength control	N/A
			6	Cooled transmitter	1		1: Cooled or Semi-cooled transmitter device	N/A
			5	Tunability	0		0: Transmitter NOT Tunable	N/A
			4	VOA implemented	0		0: Detector side VOA NOT implement	N/A
			3	Detector Type	0		01b: PIN Detector	N/A
			2		1			
			1	CDR with EDC	0		0: CDR without EDC	N/A
			0	Reserved	0		0: Reserved	N/A
801A	1	RO		Signal Code		40h	01000000	N/A
			7	Modulation	0		01b: NRZ	N/A

			6		1			
			5	Signal coding	0		0000b: Non-PSK	N/A
			4		0			
			3		0			
			2		0			
			1	Reserved	0		0: Reserved	N/A
			0		0		0: Reserved	N/A
801B	1	RO		Maximum Total Optical Output Power per Connector		70h	11220.2uW	100 uW
801C	1	RO		Maximum Optical Input Power per Network Lane		1Ch	2818.4uW	100 uW
801D	1	RO		Maximum Power Consumption		2Dh	9000mW	200 mW
801E	1	RO		Maximum Power Consumption in Low Power Mode		64h	2000mW	20 mW
801F	1	RO		Maximum Operating Case Temp Range		46h	70degC	1 degC
8020	1	RO		Minimum Operating Case Temp Range		00h	0degC	1 degC
8021	16	RO		Vendor Name				ASCII
8022								ASCII
8023								ASCII
8024								ASCII
8025								ASCII
8026								ASCII
8027								ASCII
8028								ASCII
8029								ASCII
802A								ASCII
802B								ASCII
802C								ASCII
802D								ASCII
802E								ASCII
802F								ASCII
8030								ASCII
8031	3	RO		Vendor OUI		00h		N/A

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
8034	16	RO		Vendor Part Number				ASCII
8035								ASCII
8036								ASCII
8037								ASCII
8038								ASCII
8039								ASCII
803A								ASCII
803B								ASCII
803C								ASCII
803D								ASCII
803E								ASCII
803F								ASCII
8040								ASCII
8041								ASCII
8042								ASCII
8043								ASCII
8044	16	RO		Vendor Serial Number		24h	Manufacturer serial number in ASCII code.	ASCII
8054	8	RO		Date Code		24h	Date code in YYYYMMDD	ASCII
805C	2	RO		Lot Code		24h	Lot code in ASCII code.	ASCII
805D						24h		ASCII
805E	10	RO		CLEI Code		20h	' 'in ASCII code.	ASCII
805F						20h		ASCII
8060						20h		ASCII
8061						20h		ASCII
8062						20h		ASCII
8063						20h		ASCII
8064						20h		ASCII
8065						20h		ASCII
8066						20h		ASCII
8067						20h		ASCII

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
8068	1	RO		CFP MSA Hardware Specification Revision Number		0Ah	Rev. 1.0	N/A
8069	1	RO		CFP MSA Management Interface Specification Revision Number		16h	Rev. 2.2	N/A
806A	2	RO		Module Hardware Version Number		01h	Version 1.0	N/A
806B						00h		
806C	2	RO		Module Firmware Version Number		01h	Version 1.0	N/A
806D						00h		
806E	1	RO		Digital Diagnostic Monitoring Type		0Ch	00001100	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A
			3	Received power measurement type	1		1: Averaged Power	N/A
			2	Transmitted power measurement type	1		1: Averaged Power	N/A
			1	Reserved	0		0: Reserved	N/A
			0		0		0: Reserved	N/A
806F	1	RO		DDM Capability 1		03h	00000011	N/A
			7	Transceiver auxiliary monitor 2	0		00b: Not supported	N/A
			6		0			N/A
			5	Transceiver auxiliary monitor 1	0		00b: Not supported	N/A
			4		0			N/A
			3	Reserved	0		0: Reserved	N/A
			2	Transceiver SOA Ibias monitor	0		0: Not supported	N/A
			1	Transceiver Supply voltage monitor	1		1: Supported	N/A
			0	Transceiver temperature monitor	1		1: Supported	N/A
8070	1	RO		DDM Capability 2 (per Lane)		0Eh	00001110	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
			3	Network Lane received power monitor	1		1: Supported	N/A
			2	Network Lane laser output power	1		1: Supported	N/A
			1	Network Lane laser bias current	1		1: Supported	N/A
			0	Network Lane laser temperature	0		0: Supported	N/A
8071	1	RO		Module Enhanced Options		00h	00000000	
			7	Host Lane Loop-back	0		0: Not supported	N/A
			6	Host Lane PRBS Supported	0		0: Not supported	N/A
			5	Host Lane emphasis control	0		0: Not supported	N/A
			4	Network Lane Loop-back	0		0: Not supported	N/A
			3	Network Lane PRBS	0		0: Not supported	N/A
			2	Decision Threshold Voltage control	0		0: Not supported	N/A
			1	Decision Phase control functions	0		0: Not supported	N/A
			0	Unidirectional TX/RX only Operation	0		0: Not supported	N/A
8072	1	RO		Maximum High-Power-up Time		0Ah	0Ah: 10 sec.	1 sec
8073	1	RO		Maximum TX-Turn-on Time		01h	01h: 1 sec.	1 sec
8074	1	RO		Host Lane Signal Spec		01h	01h: CAUI	N/A
8075	1	RO		Heat Sink Type		00h	00000000	N/A
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A
			5		0		0: Reserved	N/A
			4		0		0: Reserved	N/A
			3		0		0: Reserved	N/A
			2		0		0: Reserved	N/A
			1		0		0: Reserved	N/A
			0	Heat Sink Type	0		0: Flat Top	N/A
8076	1	RO		Maximum TX-Turn-off Time		96h	96h: 150 ms	1ms
8077	1	RO		Maximum High-Power-down Time		01h	01h: 1 sec.	1sec
8078	1	RO		Module Enhanced Options 2		00h	00000000	
			7	Reserved	0		0: Reserved	N/A
			6		0		0: Reserved	N/A

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Base ID Information								
			5	Host Lane Equalization control function	0		0: Reserved	N/A
			4	Active Decision Voltage and Phase Function	0		0: Not supported	N/A
			3	RX FIFO Reset	0		0: Not supported	N/A
			2	RX FIFO Auto Reset	0		0: Not supported	N/A
			1	TX FIFO Reset	0		0: Not supported	N/A
			0	TX FIFO Auto Reset	0		0: Not supported	N/A
8079	1	RO		Transmitter Monitor Clock Options		00h	00000000	
			7	1/16 of Host Lane Rate	0		0: Not supported	N/A
			6	1/16 of Network Lane Rate	0		0: Not supported	N/A
			5	1/64 of Host Lane Rate	0		0: Not supported	N/A
			4	1/64 of Network Lane Rate	0		0: Not supported	N/A
			3	Reserved	0		0: Reserved	N/A
			2	1/8 of Network Lane Rate	0		1: Supported	N/A
			1	Reserved	0		0: Reserved	N/A
			0	Monitor Clock Option	0		1: Supported	N/A
807A	1	RO		Receiver Monitor Clock Options		00h	00000000	
			7	1/16 of Host Lane Rate	0		0: Not supported	N/A
			6	1/16 of Network Lane Rate	0		0: Not supported	N/A
			5	1/64 of Host Lane Rate	0		0: Not supported	N/A
			4	1/64 of Network Lane Rate	0		0: Not supported	N/A
			3	Reserved	0		0: Reserved	N/A
			2	1/8 of Network Lane Rate	0		0: Not supported	N/A
			1	Reserved	0		0: Reserved	N/A
			0	Monitor Clock Option	0		0: Not supported	N/A
807B	1	RO		Reserved		00h	0: Reserved	N/A
807C	1	RO		Reserved		00h	0: Reserved	N/A
807D	1	RO		Maximum MDIO Ready Time		00h	0: Reserved	N/A
807E	1	RO		CFP and CFP2/4 Extended Identifer		00h	0: Reserved	N/A
807F	1	RO		CFP NVR 1 Checksum	0	00h	The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.	N/A

Table 4. CFP2 NVR 2

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Alarm/Warning Threshold Registers								
8080	2	RO		Transceiver Temp High Alarm Threshold		4Bh	75 degC	1/256 degC
8081						00h		
8082	2	RO		Transceiver Temp High Warning Threshold		46h	70degC	
8083						00h		
8084	2	RO		Transceiver Temp Low Warning Threshold		00h	0degC	
8085						00h		
8086	2	RO		Transceiver Temp Low Alarm Threshold		FBh	-5 degC	
8087						00h		
8088	2	RO		VCC High Alarm Threshold		88h	3.5V	0.1 mV
8089						B8h		
808A	2	RO		VCC High Warning Threshold		86h	3.45V	
808B						C4h		
808C	2	RO		VCC Low Warning Threshold		7Bh	3.15V	
808D						0Ch		
808E	2	RO		VCC Low Alarm Threshold		79h	3.1V	0.1 mV
808F						18h		
8090	2	RO		SOA Bias Current High Alarm Threshold		00h		
8092	2	RO		SOA Bias Current High Warning Threshold		00h		
8094	2	RO		SOA Bias Current Low Alarm Threshold		00h		
8096	2	RO		SOA Bias Current Low Warning Threshold		00h		
8098	2	RO		Auxiliary 1 monitor High Alarm Threshold		00h		
809A	2	RO		Auxiliary 1 monitor High Warning Threshold		00h		
809C	2	RO		Auxiliary 1 monitor Low Alarm Threshold		00h		
809E	2	RO		Auxiliary 1 monitor Low Warning Threshold		00h		
80A0	2	RO		Auxiliary 2 monitor High Alarm Threshold		00h		
80A2	2	RO		Auxiliary 2 monitor High Warning Threshold		00h		

80A4	2	RO		Auxiliary 2 monitor Low Alarm Threshold		00h		
80A6	2	RO		Auxiliary 2 monitor Low Warning Threshold		00h		
80A8	2	RO		Laser Bias Current High Alarm Threshold		D6h	110 mA	2uA
80A9						D8h		
80AA	2	RO		Laser Bias Current High Warning Threshold		C3h	100 mA	
80AB						50h		
80AC	2	RO		Laser Bias Current Low Warning Threshold		75h	60 mA	
80AD						30h		
80AE	2	RO		Laser Bias Current Low Alarm Threshold		61h	50 mA	
80AF						A8h		
80B0	2	RO		Laser Output Power High Alarm Threshold		DBh	7.5 dBm	0.1 uW
80B1						AAh		
80B2	2	RO		Laser Output Power High Warning Threshold		8Ah	5.5 dBm	
80B3						99h		
80B4	2	RO		Laser Output Power Low Warning Threshold		0Bh	-5.3 dBm	
80B5						87h		
80B6	2	RO		Laser Output Power Low Alarm Threshold		07h	-7.3 dBm	
80B7						46h		
80B8	2	RO		Laser Temperature High Alarm Threshold		3Ch	60 degC	1/256
80B9						00h		
80BA	2	RO		Laser Temperature High Warning Threshold		37h	55 degC	
80BB						00h		
80BC	2	RO		Laser Temperature Low Warning Threshold		1Eh	30 degC	
80BD						00h		
80BE	2	RO		Laser Temperature Low Alarm Threshold		19h	25 degC	
80BF						00h		
80C0	2	RO		Receive Optical Power High Alarm Threshold		DBh	7.5 dBm	0.1 uW
80C1						AAh		
80C2	2	RO		Receive Optical Power High Warning Threshold		9Bh	6 dBm	
80C3						82h		
80C4	2	RO		Receive Optical Power Low Warning Threshold		02h	-11.6 dBm	
80C5						B3h		
80C6	2	RO		Receive Optical Power Low Alarm Threshold		01h	-13.6 dBm	
80C7						B4h		

80C8	55	RO		Reserved		00h	0000h: Reserved	N/A
80FF	1	RO		CFP NVR 2 Checksum		24h	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.	N/A

Table 5. CFP2 NVR 3

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
Network Lane BOL Measurements								
8100	32	RO		RX Sensitivity spec for network lanes 0~15			RX Sensitivity measured in dBm @ BER=1e-12 at Typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.	0.01 dBm
8120	32	RO		Tx power spec for network lanes 0~15			TX Power measured in dBm at typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.	0.01 dBm
8140	32	RO		Measured ER for network lanes 0~15			Measured Extinction ratio at Typical condition in dB. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.	
8160	32	RO		Path Penalty for network lanes 0~15			Path penalty @worst CD at Typical condition. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.	

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Table 6. CFP2 NVR 4

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value		Description	LSB Unit
					Value	Hex		
User data registers.								
8180	1	RO	7~0	CFP NVR 3 Checksum			The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh inclusive.	N/A

8181	1	RO	7~0	Maximum OM4 Multi-Mode Optical Fiber Length		00h	8-bit value x10 m specifying maximum length of OM4 multi-mode fiber. A value of 0h is considered undefined.	10m
8182	2	RO	15~0	Extended Identifiers			MSB stored at low address. LSB stored at high address.	
			15~2	Reserved				0
			1~0	Extended Power Class			00b: Power Class 4 Module (≤ 32W max); 01b: Power Class 5 Module (≤ 64W max); 10b: Power Class 6 Module (≤ 80W max); 11b: Reserved	00b
8184	2	RO	15~0	Extended Maximum Network Lane Bit Rate			Unsigned 16-bit value x 0.1 Gbps. MSB stored at low address. LSB stored at high address.	
8186	2	RO	15~0	Extended Maximum Power Consumption			Unsigned 16-bit value x 10 mW. MSB stored at low address. MSB stored at low address. LSB stored at high address.	
8188	2	RO	15~0	Extended Maximum Power Consumption in Low Power			Unsigned 16-bit value x 1 mW. MSB stored at low address. LSB stored at high address.	
818A	2	RO	15~0	TX/RX Minimum Laser Frequency 1			An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address	
818C	2	RO	15~0	TX/RX Minimum Laser Frequency 2			An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB stored at low address. LSB stored at high address.	
818E	2	RO	15~0	TX/RX Maximum Laser Frequency 1			An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address.	
8190	2	RO	15~0	TX/RX Maximum Laser Frequency 2			An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB	

							stored at low address. LSB stored at high address.	
8192	2	RO	15~0	RX Laser Fine Tune Frequency Range (FTF) (Optional)			An unsigned 16-bit integer with LSB = 1 MHz. The range covers the min/max range symmetrically about 0. Set to zero if FTF is not supported. MSB stored at low address. LSB stored at high address.	
8194	2	RO	15~0	TX Laser Fine Tune Frequency Range (FTF) (Optional)			An unsigned 16-bit integer with LSB = 1 MHz. The range covers the min/max range symmetrically about 0. Set to zero if FTF is not supported. MSB stored at low address. LSB stored at high address.	
8196	2	RO	15~0	Laser Tuning Capabilities			MSB stored at low address. LSB stored at high address.	
			15	6.25 GHz Grid Spac			1 = Supported, 0 = Not Supported	
			14	12.5 GHz Grid Spacing			1 = Supported, 0 = Not Supported	
			13	25 GHz Grid Spacing			1 = Supported, 0 = Not Supported	
			12	33 GHz Grid Spacing			1 = Supported, 0 = Not Supported	
			11	50 GHz Grid Spacing			1 = Supported, 0 = Not Supported	
			10	100 GHz Grid Spacing			1 = Supported, 0 = Not Supported	
			9~0	Maximum Channels			Maximum channels supported based on minimum grid spacing supported	
8198	8	RO	7~0	Reserved				
81A0	8	RO	7~0	Network Lane n Vendor Specific Auxiliary 1 Monitor Thresholds			Definition provided by vendor, related to A340. For MSA 100GLH module, related to B140h.	
81A8	8	RO	7~0	Network Lane n Vendor Specific Auxiliary 2 Monitor Thresholds			Definition provided by vendor, related to A350. For MSA 100GLH module, related to B150h.	
81B0	8	RO	7~0	Network Lane n Vendor Specific Auxiliary 3 Monitor Threshold			Definition provided by vendor, related to A360. For MSA 100GLH module, related to B160h.	
81B8	8	RO	7~0	Network Lane n Vendor			Definition provided by vendor,	

				Specific Auxiliary 4 Monitor Threshold			related to A370. For MSA 100GLH module, related to B170h	
81C0	6	RO		Reserved for Future Host Lane Signal Mode Bit Map Support				
81C6	1	RO		Host Lane Signal Mode Bit Map 1				
			7~5	Reserved				
			4	OTL10.4			1: OTL10.4 supported, 0: OTL10.4 not supported	
			3	OTL3.4			1: OTL3.4 supported, 0: OTL3.4 not supported	
			2	OTL4.4			1: OTL4.4 supported, 0: OTL4.4 not supported	
			1	MLG2.0			1: MLG2.0 supported, 0: MLG2.0 not supported	
			0	MLG1.1			1: MLG1.1 supported, 0: MLG1.1 not supported	
81C7	1	RO		Host Lane Signal Mode Bit Map 0				
			7	MLG1.0			1: MLG1.0 supported, 0: MLG1.0 not supported.	
			6	CPPI			1: CPPI supported, 0: CPPI not supported	
			5	CEI-28G VSR			1: CEI-28G VSR supported, 0: CEI-28G VSR not supported	
			4	CAUI-4f			1: CAUI-4f supported, 0: CAUI-4f not supported	
			3	CAUI-4			1: CAUI-4 supported, 0: CAUI-4 not supported	
			2	SFI5.2			1: SFI5.2 supported, 0: SFI5.2 not supported	
			1	XLAUI			1: XLAUI supported, 0: XLAUI not supported	
			0	CAUI			1: CAUI supported, 0: CAUI not supported	
81C8	47	RO		Reserved				
81FF	1	RO	7~0	CFP NVR 4 Checksum			The 8-bit unsigned sum of all CFP NVR 4 contents from address 8181h through 81FEh inclusive.	

Table 7. CFP2 Module VR 1

CFP Module VR 1						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
Module Command/Setup Registers						
A000	2	WO	15~0	Password Entry(Optional)	Password for module registers access control. Two word value. MSW is in the lower address. Reading these registers always returns FFFFh.	0000h 0000h
A002	2	WO	15~0	Password Change (Optional)	New password entry. Two word value. MSW is in the lower address. Reading these registers always returns FFFFh.	0000h 0000h
A004	1			NVR Access Control	User NVRs Restore/Save command. Refer to 4.10.2 for details.	0000h
		RW	15~9	Reserved	Vendor specific.	0
		RO	8~6	Reserved		000b
		RW	5	User Restore and Save Command	0: Restore the User NVR section, 1: Save the User NVR section.	0
		RO	4	Reserved		0
		RO	3~2	Command Status	00b: Idle, 01b: Command completed successfully, 10b: Command in progress, 11b: Command failed.	00b
		RW	1~0	Extended Commands	00b: No effect, 01b: Vendor Specific, 10b: Vendor Specific, 11b: Restore/Save the User NVRs.	00b
A005	1			PRG_CNTL3 Function Select	Selects, and assigns, a control function to PRG_CNTL3.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A006	1			PRG_CNTL2 Function Select	Selects, and assigns, a control function to PRG_CNTL2.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward.	00h

					0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	
A007	1			PRG_CNTL1 Function Select	Selects, and assigns, a control function to PRG_CNTL1.	0001h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC RSTn is the CFP MSA default function for PRG_CNTL1. 2~255: Reserved.	01h
A008	1			PRG_ALRM3 Source Select	Selects, and assigns, an alarm source for PRG_ALRM3.	0003h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, 3: Fault State, MSA default setting, 4: RX ALRM = RX LOS + RX NETWORK LOL, 5: TX ALRM = TX LOSF + TX HOST LOL + TX_CMU_LOL, 6: RX NETWORK LOL, 7: TX LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and shall be read as 0. This is also true for Registers A009h and A00Ah). 10~255: Reserved.	03h
A009	1			PRG_ALRM2 Source Select	Selects, and assigns, an alarm source for PRG_ALRM2.	0002h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, MSA default setting, 3: Fault State, 4: RX ALRM = RX LOS + RX NETWORK LOL, 5: TX ALRM = TX LOSF + TX HOST LOL + TX_CMU_LOL, 6: RX NETWORK LOL, 7: TX LOSF,	02h

					8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	
A00A	1			PRG_ALRM1 Source Select	Selects, and assigns, an alarm source for PRG_ALRM1.	0001h
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX ALRM = RX LOS + RX NETWORK LOL, 5: TX ALRM = TX LOSF + TX HOST LOL + TX CMU LOL, 6: RX NETWORK LOL, 7: TX LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	01h
A00B	1			Module Bi-/Uni-Directional Operating Mode Select		0000h
		RO	15~3	Reserved		0
		RW	2~0	Module Bi/uni-direction mode Select	000b: Normal bi-directional mode,	
A00C	4	RO		Reserved		0000h
Module Control Registers						
A010	1			Module General Control		0000h
		RW/SC/LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0

		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		RO	8~6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD LOPWR Pin State	Logical state of the MOD_LOPWR pin.	
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin. 1: Assert.	0
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Assert.	0
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin. 1: Assert.	0
		RO	0	Reserved		0
A011	1			Network Lane TX Control	This control acts upon all the network lanes.	0000h
		RO	15	Reserved		0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00b:2^7,	00b
		RW	12	TX PRBS Pattern 0	01b:2^{15}, 10b:2^{23}, 11b:2^{31}.	
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	0
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW	7~5	TX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RO	4	Reserved		0b
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b
A012	1			Network Lane RX Control	This control acts upon all the network lanes.	0000h
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module.	RW
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13	RX PRBS Pattern 1	00b: 2^7,	00b

		RW	12	RX PRBS Pattern 0	01b: 2^{15}, 10b: 2^{23}, 11b: 2^{31}.	
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	0b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW	7~5	RX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b
A013	1			Individual Network Lane TX_DIS Control	This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state	0000h
		RW	15	Lane 15 Disable	0: Normal, 1: Disable.	0
		RW	14	Lane 14 Disable	0: Normal, 1: Disable.	0
		RW	13	Lane 13 Disable	0: Normal, 1: Disable.	0
		RW	12	Lane 12 Disable	0: Normal, 1: Disable.	0
		RW	11	Lane 11 Disable	0: Normal, 1: Disable.	0
		RW	10	Lane 10 Disable	0: Normal, 1: Disable.	0
		RW	9	Lane 9 Disable	0: Normal, 1: Disable.	0
		RW	8	Lane 8 Disable	0: Normal, 1: Disable.	0
		RW	7	Lane 7 Disable	0: Normal, 1: Disable.	0
		RW	6	Lane 6 Disable	0: Normal, 1: Disable.	0
		RW	5	Lane 5 Disable	0: Normal, 1: Disable.	0
		RW	4	Lane 4 Disable	0: Normal, 1: Disable.	0
		RW	3	Lane 3 Disable	0: Normal, 1: Disable.	0
		RW	2	Lane 2 Disable	0: Normal, 1: Disable.	0
		RW	1	Lane 1 Disable	0: Normal, 1: Disable.	0
		RW	0	Lane 0 Disable	0: Normal, 1: Disable.	0
				Host Lane Control	This control acts upon all the host lanes.	0000h

CFP Module VR 1						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
A014	1	RO	15	Reserved		0
		RW	14	TX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 2	000b:2^7, 100b:2^23, 001b: 2^9, 101b: reserved, 010b:2^15, 110b:2^31, 011b: reserved, 111b: reserved.	000b
		RW	12	TX PRBS Pattern 1		
		RO	11	TX PRBS Pattern 0		
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)	0
		RO	9	Reserved		0
		RO	8	Reserved		0
		RW	7	RX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	5	RX PRBS Pattern 0		
		RO	4~0	Reserved		0h
A015	1	RW		Module General Control 2	This register collects added module general control functions for CFP MSA MIS V2.2	0000h
			15	Enable Tx Network Lane PRBS Modes.	Enables standard or extended Tx Network Lane PRBS Modes in Register A011. 0: Enable standard modes, 1: Enable extended modes.	
			14	Enable Rx Network Lane PRBS Modes.	Enables standard or extended Rx Network Lane PRBS Modes in Register A012. 0: Enable standard modes, 1: Enable extended modes.	
			13~12	MCLK Selection (CFP2)	Selects the source of the MCLK for CFP2 modules. 00b: MCLK Off 01b: MCLK = TX_MCLK 10b: MCLK = RX_MCLK 11b: Reserved.	
			11	Tx Lane Offset Enable	Optional feature to enable delaying Tx Lanes by 32 bytes to prevent frame alignment bytes from overlapping. 0: Disabled, 1: Enabled	
			10	Rx Lane Offset Enable	Optional feature to enable delaying Rx Lanes by 32 bytes to revent frame alignment bytes from overlapping. 0: Disabled, 1: Enabled	
			9	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h~80C7h, 1: Host Configured Receive Optical Power Threshold registers A03Ch~A03Fh.	
			8	Reserved		
			7~0	Electrical Interface Format Select (Optional)	Host writes to select in which mode the module should operate. 00h: Unspecified,01h: CAUI,02h: XLAUI,03h: SFI5.2,04h: SFI-S,05h: OTL3.4,06h: OTL4.10,07h: OTL4.4,08h: STL256.4,09h: CPPI,0Ah: CAUI-4,0Bh:	

					CAUI-4f,0Ch: CEI-28G VSR,0Dh: MLG1.0,0Eh: MLG1.1,0Fh: MLG2.0,10h~FFh: Reserved	
Module State Register						
A016	1			Module State	CFP module state. Only a single bit set at any time	0000h
		RO	15~9	Reserved		0
		RO	8	High-Power-down State	1: Corresponding state is active. Word value = 0100h.	0
		RO	7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
		RO	6	Fault State	1: Corresponding state is active. Word value = 0040h.	0
		RO	5	Ready State	1: Corresponding state is active. Word value = 0020h. (Also referred to as MOD_READY)	0
		RO	4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0
		RO	3	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
		RO	2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0
		RO	1	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
		RO	0	Initialize State	1: Corresponding state is active. Word value = 0001h.	0
Module Alarm Summary Registers						
A017	1	RO		Reserved		0000h
		RO		Global Alarm Summary		
		RO	15	GLB_ALRM Assertion Status	Internal status of global alarm output. 1: Asserted.	0
A018	1	RO	14	Host Lane Fault and Status Summary	Logical OR of all the enabled bits of Host Lane Fault and Status Summary register.	0
		RO	13	Network Lane Fault and Status Summary	Logical OR of all the bits in the Network Lane Fault and Status Summary register.	0
		RO	12	Network Lane Alarm and Warning Summary	Logical OR of all the bits in the Network Lane Alarm and Warning Summary register.	0
		RO	11	Module Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Module Alarms and Warnings 2 Latch register.	0
		RO	10	Module Alarm and Warning 1 Summary	Logical OR of all the enabled bits of Module Alarms and Warnings 1 Latch register.	0
		RO	9	Module Fault Summary	Logical OR of all the enabled bits of Module Fault Status Latch register.	0
		RO	8	Module General Status Summary	Logical OR of all the enabled bits of Module General Status Latch register.	0
		RO	7	Module State Summary	Logical OR of all the enabled bits of Module State Latch register.	0
		RO	6~1	Reserved		0
		RO	0	Soft GLB_ALRM Test Status	Soft GLB_ALRM Test bit Status.	0
A019	1	RO		Network Lane Alarm and Warning Summary	Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning Latch registers.	0000h
		RO	15	Lane 15 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 15 Network Lane Alarm and Warning Register. 1=Fault	0

					asserted.	
		RO	14	Lane 14 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 14 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	13	Lane 13 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 13 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	12	Lane 12 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 12 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	11	Lane 11 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 11 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	10	Lane 10 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 10 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	9	Lane 9 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 9 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	8	Lane 8 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 8 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	7	Lane 7 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 7 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	6	Lane 6 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 6 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	5	Lane 5 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 5 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	4	Lane 4 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 4 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	3	Lane 3 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 3 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	2	Lane 2 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 2 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	1	Lane 1 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 1 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO	0	Lane 0 Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane 0 Network Lane Alarm and Warning Register. 1=Fault asserted.	0
		RO		Network Lane Fault and Status Summary	Each bit is the logical OR of all enabled bits in each of the Network Lane fault and Status Latch registers.	0000h
		RO	15	Lane 15 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 15 Network Lane Fault and Status Register. 1 =Fault	0

					asserted.	
		RO	14	Lane 14 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 14 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	13	Lane 13 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 13 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	12	Lane 12 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 12 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	11	Lane 11 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 11 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	10	Lane 10 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 10 Network Lane Fault and Status Register. 1 =Fault asserted.	0
A01A	1	RO	9	Lane 9 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 9 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	8	Lane 8 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 8 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	7	Lane 7 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 7 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	6	Lane 6 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 6 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	5	Lane 5 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 5 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	4	Lane 4 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 4 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	3	Lane 3 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 3 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	2	Lane 2 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 2 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	1	Lane 1 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 1 Network Lane Fault and Status Register. 1 =Fault asserted.	0
		RO	0	Lane 0 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 0 Network Lane Fault and Status Register. 1 =Fault asserted.	0
A01B	1	RO		Host Lane Fault and Status Summary	Each bit is the logical OR of all enabled bits in each of the Host Lane fault and Status Latch registers	0000h
		RO	15	Lane 15 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 15 Host Lane Fault and Status Register. 1=Fault asserted.	0

		RO	14	Lane 14 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 14 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	13	Lane 13 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 13 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	12	Lane 12 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 12 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	11	Lane 11 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 11 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	10	Lane 10 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 10 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	9	Lane 9 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 9 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	8	Lane 8 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 8 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	7	Lane 7 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 7 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	6	Lane 6 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 6 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	5	Lane 5 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 5 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	4	Lane 4 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 4 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	3	Lane 3 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 3 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	2	Lane 2 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 2 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	1	Lane 1 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 1 Host Lane Fault and Status Register. 1=Fault asserted.	0
		RO	0	Lane 0 Fault and Status Summary	Logical OR of all enabled bits in Latched Lane 0 Network Lane Fault and Status Register. 1 =Fault asserted.	0
A01C	1	RO		Reserved		0
Module FAWS Registers						
A01D	1			Module General Status		0000h
		RO	15	Reserved		0
		RO	14	Reserved		0
		RO	13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity	0
		RO	12~11	Reserved		0
		RO	10	Loss of REFCLK Input	Loss of reference clock input. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of signal	0
		RO	9	TX_JITTER_PLL_LOL	TX jitter PLL loss of lock. It is an optional feature. (FAWS_TYPE_B).	0

					0: Normal, 1: Loss of lock	
		RO	8	TX_CMU_LOL	TX CMU loss of lock. It is the loss of lock indicator on the network side of the CMU. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
		RO	7	TX_LOSF	Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX LOSF bits. PRG ALRMx mappable. . (FAWS_TYPE_C, since the TX must be enabled). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 -- > 0) of this status signal. 0: all transmitter signals functional, 1: any transmitter signal not functional.	0
		RO	6	TX_HOST_LOL	TX IC Lock Indicator. Logic OR of all host lane TX LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal. 0: Locked, 1: Loss of lock.	0
		RO	5	RX_LOS	Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal. 0: No network lane RX_LOS bit asserted, 1: Any network lane RX_LOS bit asserted.	0
		RO	4	RX_NETWORK_LOL	RX IC Lock Indicator. Logic OR of all network lane RX LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal. 0: Locked, 1: Loss of lock.	0
		RO	3	Out of Alignment	Host lane skew out of alignment indicator. Applicable only for some internal implementations. (FAWS_TYPE_B). 0: Normal, 1: Out of alignment.	0
		RO	2	Reserved		0
		RO	1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status, 1: Module is in high powered on status.	0
		RO	0	Reserved		0
				Module Fault Status	Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.	0000h

		RO	15	Reserved	Reserved for extension of “other faults” in case of all the bits used up in this register.	0
A01E	1	RO	14~7	Reserved		0
		RO	6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
		RO	5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
		RO	4~2	Reserved		000b
		RO	1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
		RO	0	Reserved		0
A01F	1			Module Alarms and Warnings 1		0000h
		RO	15~12	Reserved		0000b
		RO	11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
		RO	4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TY PE_A) 0: Normal, 1: Asserted.	0
		RO	3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		RO	2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		RO	1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
		RO	0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
				Module Alarms and Warnings 2		0000h
		RO	15~8	Reserved		0
		RO	7	Mod Aux 1 High Alarm	Module aux ch 1 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted..	0
		RO	6	Mod Aux 1 High Warning	Module aux ch 1 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		RO	5	Mod Aux 1 Low Warning	Module aux ch 1 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
A020	1	RO	4	Mod Aux 1 Low Alarm	Module aux ch 1 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0

		RO	3	Mod Aux 2 High Alarm	Module aux ch 2 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		RO	2	Mod Aux 2 High Warning	Module aux ch 2 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		RO	1	Mod Aux 2 Low Warning	Module aux ch 2 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
		RO	0	Mod Aux 2 Low Alarm	Module aux ch 2 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
A021	1	RO		Reserved		0
Module FAWS Latch Registers						
A022	1			Module State Latch	CFP module state Latch.	0000h
		RO	15~9	Reserved		0
		RO/LH/COR	8	High-Power-down State Latch	1: Latched.	0
		RO/LH/COR	7	TX-Turn-off State Latch	1: Latched.	0
		RO/LH/COR	6	Fault State Latch	1: Latched.	0
		RO/LH/COR	5	Ready State Latch	1: Latched.	0
		RO/LH/COR	4	TX-Turn-on State Latch	1: Latched.	0
		RO/LH/COR	3	TX-Off State Latch	1: Latched.	0
		RO/LH/COR	2	High-Power-up State Latch	1: Latched.	0
		RO/LH/COR	1	Low-Power State Latch	1: Latched.	0
		RO/LH/COR	0	Initialize State Latch	1: Latched.	0
A023	1			Module General Status Latch		0000h
		RO	15	Reserved		0
		RO	14	Reserved		0
		RO/LH/COR	13	HW Interlock Latch	1: Latched.	0
		RO	12~11	Reserved		0
		RO/LH/COR	10	Loss of REFCLK Input Latch	1: Latched.	0
		RO/LH/COR	9	TX_JITTER_PLL_LOL	1: Latched.	0
		RO/LH/COR	8	TX CMU LOL Latch	1: Latched.	0
		RO/LH/COR	7	TX_LOSF Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	6	TX_HOST_LOL Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	5	RX_LOS Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0

		RO/LH/COR	4	RX_NETWORK_LOL Latch	1: Latched. Note: Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	3	Out of Alignment Latch	1: Latched.	0
		RO	2~0	Reserved		000b
A024	1			Module Fault Status Latch	Module Fault Status latched bit pattern.	0000h
		RO	15~7	Reserved		0
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	1: Latched.	0
		RO/LH/COR	5	Power Supply Fault Latch	1: Latched.	0
		RO	4~2	Reserved		000b
		RO/LH/COR	1	CFP Checksum Fault Latch	1: Latched.	0
		RO	0	Reserved		0
A025	1			Module Alarms and Warnings 1 Latch		0000h
		RO	15~12	Reserved		0000b
		RO/LH/COR	11	Mod Temp High Alarm Latch	1: Latched.	0
		RO/LH/COR	10	Mod Temp High Warning Latch	1: Latched.	0
		RO/LH/COR	9	Mod Temp Low Warning Latch	1: Latched.	0
		RO/LH/COR	8	Mod Temp Low Alarm Latch	1: Latched.	0
		RO/LH/COR	7	Mod Vcc High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Mod Vcc High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Vcc Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Vcc Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	Mod SOA Bias High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch	1: Latched.	0
A026	1			Module Alarms and Warnings 2 Latch		0
		RO	15~8	Reserved		0
		RO/LH/COR	7	Mod Aux 1 High Alarm	1: Latched.	0

				Latch		
		RO/LH/COR	6	Mod Aux 1 High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	1: Latched.	0
A027	1	RO		Reserved		0
Module FAWS Enable Registers						
A028	1			Module State Enable	GLB_ALRM Enable register for Module State change. One bit for each state.	0000h
		RO	15~9	Reserved		0
		RW	8	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	7	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	6	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	0
		RW	5	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	0
		RW	4	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	3	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	0
		RW	2	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	1	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence)	0
		RO	0	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
A029	1			Module General Status Enable	1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.	A1B0h

		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW Interlock	1: Enable.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	0
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	0
		RW	8	TX CMU LOL Enable	1: Enable.	1
		RW	7	TX LOSF Enable	1: Enable.	1
		RW	6	TX HOST LOL Enable	1: Enable.	0
		RW	5	RX LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	0
		RO	2~0	Reserved		000b
				Module Fault Status Enable	These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	0002h
		RO	15~7	Reserved		0
A02A	1	RW	6	PLD or Flash Initialization Fault Enable		0
		RW	5	Power Supply Fault Enable		0
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable		1
		RO	0	Reserved		0
A02B	1			Module Alarm and Warnings 1 Enable	These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	0FF0h
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
		RW	10	Mod Temp Hi Warn Enable	1: Enable.	1
		RW	9	Mod Temp Low Warning Enable	1: Enable.	1
		RW	8	Mod Temp Low Alarm Enable	1: Enable.	1

		RW	7	Mod Vcc High Alarm Enable	1: Enable.	1
		RW	6	Mod Vcc High Warning Enable	1: Enable.	1
		RW	5	Mod Vcc Low Warning Enable	1: Enable.	1
		RW	4	Mod Vcc Low Alarm Enable	1: Enable.	1
		RW	3	Mod SOA Bias High Alarm Enable	1: Enable.	0
		RW	2	Mod SOA Bias High Warning Enable	1: Enable.	0
		RW	1	Mod SOA Bias Low Warning Enable	1: Enable.	0
		RW	0	Mod SOA Bias Low Alarm Enable	1: Enable.	0
				Module Alarms and Warnings 2 Enable	These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 2 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	0000h
		RO	15~8	Reserved		00h

CFP Module VR 1						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
A02C	1	RW	7	Mod Aux 1 High Alarm Enable	1: Enable.	0
		RW	6	Mod Aux 1 High Warning Enable	1: Enable.	0
		RW	5	Mod Aux 1 Low Warning Enable	1: Enable.	0
		RW	4	Mod Aux 1 Low Alarm Enable	1: Enable.	0
		RW	3	Mod Aux 2 High Alarm Enable	1: Enable.	0
		RW	2	Mod Aux 2 High Warning Enable	1: Enable.	0
		RW	1	Mod Aux 2 Low Warning Enable	1: Enable.	0
		RW	0	Mod Aux 2 Low Alarm Enable	1: Enable.	0
A02D	2	RO		Reserved		0000h
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between -40 and	0000h

					+125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	
A030	1	RO	15~0	Module Power supply 3.3 V Monitor A/D Value	Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 0.1 mV, yielding a total measurement range of 0 to 6.5535 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.	0000h
A031	1	RO	15~0	SOA Bias Current A/D Value	Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/-10% of the nominal value over specified temperature and voltage.	0000h
A032	1	RO	15~0	Module Auxiliary 1 Monitor A/D Value	Definition depending upon the designated use.	0000h
A033	1	RO	15~0	Module Auxiliary 2 Monitor A/D Value	Definition depending upon the designated use.	0000h
A034	4	RO		Reserved		
A038	1			Network Lane PRBS Data Bit Count	Network lane data bit counter increments when network lane RX PRBS Checker is enabled. It stops counting when RX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.	0000h
		RO	15~10	Exponent	6-bit unsigned exponent.	0
		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
A039	1			Host Lane PRBS Data Bit Count	Host lane data bit counter increments when host side TX PRBS Checker is enabled. It stops counting when TX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.	0000h
		RO	15~10	Exponent	6-bit unsigned exponent	0
		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
A03A	70	RO		Reserved		0

Table 8 Network Lane VR 1

Table 8 Network Lane VR 1 and Table 9 Network Lane VR 2 contain network lane specific registers. Each register listed is the nth element of a 16-register array, representing the nth network lane of N total network lanes. The maximum N CFP MSA specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

Network Lane VR 1						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
Network Lane FAWS Registers						
A200	16			Network Lane n Alarm and Warning	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1 N-1. N_max = 16. Actual N is module dependent.	0000h
		RO	15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
A210	16			Network Lane n Fault and Status	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	0000h
		RO	15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
		RO	13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	12~8	Reserved		0
		RO	7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
		RO	6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
		RO	5	Reserved		0
		RO	4	Lane RX LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

		RO	3	Lane RX LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
		RO	2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
		RO	1	Reserved.		0
		RO	0	Reserved.		0
Network Lane FAWS Latch Registers						
A220	16			Network Lane n Alarm and Warning Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	0000h
		RO/LH/COR	15	Bias High Alarm Latch	1: Latched.	0
		RO/LH/COR	14	Bias High Warning Latch	1: Latched.	0
		RO/LH/COR	13	Bias Low Warning Latch	1: Latched.	0
		RO/LH/COR	12	Bias Low Alarm Latch	1: Latched.	0
		RO/LH/COR	11	TX Power High Alarm Latch	1: Latched.	0
		RO/LH/COR	10	TX Power High Warning Latch	1: Latched.	0
		RO/LH/COR	9	TX Power Low Warning Latch	1: Latched.	0
		RO/LH/COR	8	TX Power Low Alarm Latch	1: Latched.	0
		RO/LH/COR	7	Laser Temperature High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Laser Temperature High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Laser Temperature Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Laser Temperature Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	RX Power High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	RX Power High Warning Latch	1: Latched.	0
		RO/LH/COR	1	RX Power Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	RX Power Low Alarm Latch	1: Latched.	0
A230	16			Network Lane n Fault and Status Latch	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	
		RO/LH/COR	15	Lane TEC Fault Latch	1: Latched.	0
		RO/LH/COR	14	Lane Wavelength Unlocked Fault Latch	1: Latched.	0
		RO/LH/COR	13	Lane APD Power Supply Fault Latch	1: Latched.	0

		RO/LH/COR	12~8	Reserved		0
		RO/LH/COR	7	Lane TX_LOSF Latch	1: Latched.	0
		RO/LH/COR	6	Lane TX_LOL Latch	1: Latched.	0
		RO/LH/COR	5	Reserved		0
		RO/LH/COR	4	Lane RX_LOS Latch	1: Latched.	0
		RO/LH/COR	3	Lane RX_LOL Latch	1: Latched.	0
		RO/LH/COR	2	Lane RX FIFO Status Latch	1: Latched.	0
		RO/LH/COR	1~0	Reserved		0
Network Lane FAWS Enable Registers						
A240	16			Network Lane n Alarm and Warning Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	FFFFh
		RW	15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
		RW	14	Bias High Warning Enable	0: Disable, 1: Enable.	1
		RW	13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
		RW	12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
		RW	11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
		RW	10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
		RW	9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
		RW	8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
		RW	7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
		RW	6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
		RW	5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
		RW	4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
		RW	3	RX Power High Alarm Enable	0: Disable, 1: Enable.	1
		RW	2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
		RW	1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
		RW	0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1
A250	16			Network Lane n Fault and Status Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	E0D8h

		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RO	1~0	Reserved		0
A260	32	RO		Reserved		0000h

Table 9 Network Lane VR 2

Network Lane VR 2						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
Network Lane Control Registers						
A280	16			Network Lane n FEC Controls	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent.	0000h
		RW	15~8	Phase Adjustment	This signed 8-bit value represents the phase set point of receive path quantization relative to 0.5 UI, given by: 0.5UI + (Phase Adjustment) / 256 UI. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
		RW	7~0	Amplitude Adjustment	This signed 8-bit value represents the amplitude threshold of relative amplitude of receive path quantization relative to 50% (Optional function), given by: 50% + (Amplitude Adjustment) / 256 * 100%. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
A290	16			Network Lane n PRBS Rx Error Count	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent. This counter increases upon detection of each network lane RX checker error when RX PRBS Checker is enabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa. Base of exponent is 2 and Mantissa radix is 0.	0000h
		RO	15~10	Exponent	6-bit unsigned exponent.	0

		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Network Lane A/D value Measurement Registers						
A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.	0000h
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent. Measured TX output power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a range of laser output power from 0 to 6.5535 mW (-40 to +8.2 dBm). Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	0000h
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between -40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.	0000h
A2E0	32	RO	15~0	Reserved		0000h

Table 10 Host Lane VR 1

Table 10 Host Lane VR 1 contains host lane specific registers. Each register listed is the mth element of a 16-register array, representing the mth host lane of M total host lanes. The maximum M CFP MSA

specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

Host Lane VR 1						
Hex Addr.	**Size**	**Access Type**	**Bit**	**Register Name Bit Field Name**	**Description**	**Init Value**
Host Lane FAWS Status Registers						
A400	16			Host Lane m Fault and Status	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …,M-1. M_max = 16. Actual M is module dependent.	0000h
		RO	15~2	Reserved		0
		RO	1	Lane TX FIFO Error	Lane specific TX FIFO error. (FAWS_TYPE_B) 0: Normal, 1: Error.	0
		RO	0	TX_HOST_LOL	TX IC Lock Indicator, (FAWS_TYPE_B) 0: Locked,	0
Host Lane FAWS Latch Registers						
A410	16			Host Lane m Fault and Status Latch	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …,M-1. M_max = 16. Actual M is module dependent.	0000h
		RO	15~2	Reserved		0
		RO/LH/COR	1	Lane TX FIFO Error Latch	1: Latched.	0
		RO/LH/COR	0	TX_HOST_LOL Latch	1: Latched.	0
Host Lane FAWS Enable Registers						
A420	16			Host Lane m Fault and Status Enable	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …,M-1. M_max = 16. Actual M is module dependent.	0001h
		RO	15~2	Reserved		0
		RW	1	Lane TX FIFO Error Enable	1: Enable.	0
		RW	0	TX HOST LOL Enable	1: Enable.	1
Host Lane Digital PRBS Registers						
A430	16			Host Lane m PRBS TX Error Count	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …,M-1. M_max = 16. Actual M is module dependent. This counter increases upon detection of each RX checker error when host lane TX PRBS checker is enabled. It stops counting when the TX PRBS checker is disabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	0000h
		RO	15~10	Exponent	6-bit unsigned exponent.	0
		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0

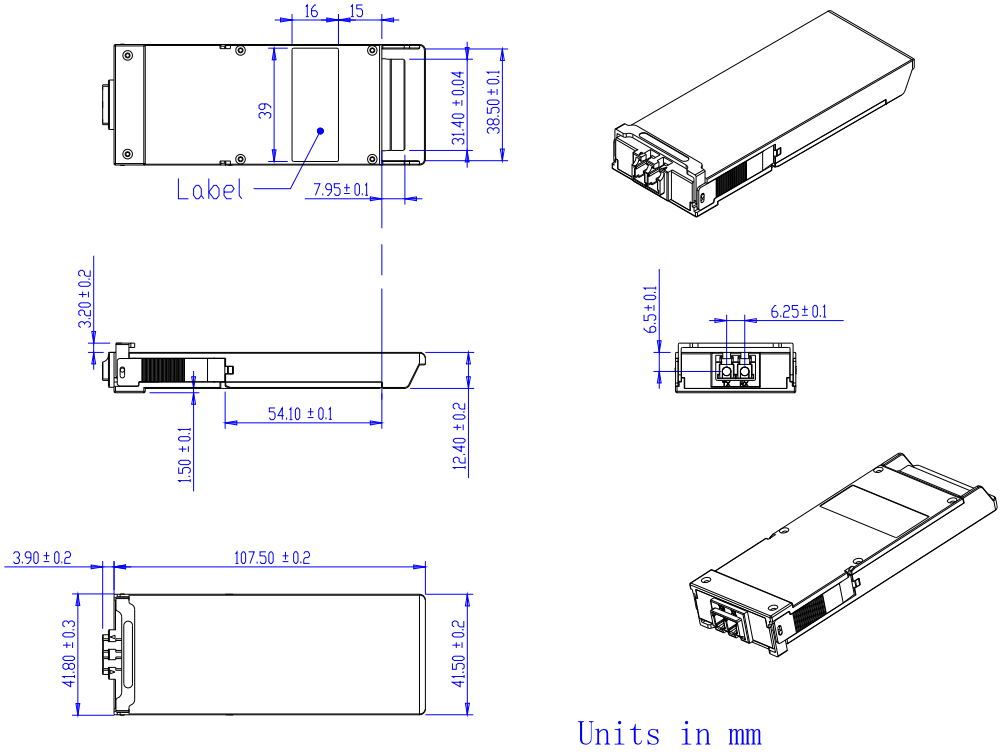
Host Lane Control Registers						
A440	16			Host Lane m Control	16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …,M-1. M_max = 16. Actual M is module dependent.	0007h
		RO	15~4	Reserved		0
		RW	3~0	Signal Pre/De-emphasis	4-bit unsigned number N represents the pre/de¬emphasis applied. Pre/De-emphasis = N * 0.5 dB, N = 0, ..., 15. The power on default is 3.5 dB with a value of 7 in this field.	7
A450	48	RO		Reserved		0000h

V. Optical Receiver Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Signaling rate, each lane			25.78125		GBd	
Rate tolerance		-100		100	ppm	From normal rate
Average receive power, each lane	Pavg	-10.6		4.5	dBm	
Receive power, each lane (OMA)				4.5	dBm	
Difference in launch power between any two lanes (OMA)				5.5	dB	
Receiver Sensitivity (OMA), each lane	Rsen			-8.6	dBm	1
Stressed Receiver Sensitivity (OMA), each lane	SRS			-6.8	dBm	
Stressed receiver sensitivity test conditions						
Vertical eye closure penalty, each lane	VECP		1.8		dB	
Stressed sys J2 jitter, each lane	J2		0.3		UI	2
Stressed sys J9 jitter, each lane	J9		0.47		UI	2
Receiver reflectance				-26	dB	
LOS Assert	Plos_on	-30			dBm	
LOS Deassert	Plos_off			-12	dBm	
LOS Hysteresis		0.5		4	dB	

1. Receiver sensitivity (OMA), each lane, is informative.
2. Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

VI. Outline Dimensions



Appendix A. Document Revision

Version No.	Date	Description
Preliminary	2015-4-13	Preliminary datasheet